Code No.: **54306**

MR 15

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.-500 100.

M.TECH II SEMESTER REGULAR END EXAMINATIONS, JULY-2017

SUBJECT: **EMBEDDED NETWORKING**

Branch/Specialization: ECE/Embedded Systems

Time: **3 Hours** Max Marks: **60**

PART-A

Answer the following Questions **5 X 4 Marks=20 Marks**

1) Mention some serial communication protocols? (4M)
2) What is CAN ? How many types of errors may occur in CAN. what are they. (4M)
3) Explain Multilevel Transition 3 (MLT-3)encoding? (4M)
4) Write a note on net media site player Ethernet web-server ? (4M)
5) What are the limitations of multilateration technique ? (4M)

PART-B

Answer any 5 questions **5 X 8 Marks=40 Marks**

1. Draw and Explain timing diagram of serial peripheral interface and RS485 (8M)
2. Write a short notes on a) USB enumeration b) encoding techniques in Media Systems (8M)
3. a) Explain the working of an Ethernet controller? (4M)
   b) Explain frame format of UDP header? (4M)
4. Explain sensor MAC. (8M)
5. What is Geographic routing and explain (8M)
6. a) Write a short notes on AES encryption. (4M)
   b) Write a short notes on Virtual private networks. (4M)
7. a. Explain about different states in USB. (4M)
   b. Explain the ethenet protocol analyzer? (4M)
8. Write Short notes on any **two** of the following
   a. List any five commands of POP3 Standard? (4M)
   b. A server side include directives? (4M)
   c. Explain localization (4M)

Code No.: **54115**

MR 15 – 2015-16 (Supply) & 2016-17 (Regular) Admitted Students

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.-500 100.

M.TECH II SEMESTER REGULAR & SUPPLEMENTARY EXAMINATIONS, JULY-2017

SUBJECT: **DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES**

Branch/Specialization: **ECE/ Common Embedded Systems & DS& CE**

Time: **3 Hours** Max Marks: **60**

PART-A

Answer the following Questions **5 X 4 Marks=20 Marks**

1. Why signal sampling is required? Explain the sampling process.
2. With neat diagram explain multiply & Accumulate unit of DSP system?
3. Why circular buffers are required in DSP processor? How they are implemented?
4. Draw a neat block diagram of ADSP 2100 Processor.
5. What are interrupts? How interrupts are handled by C54xx DSP Processors.

PART-B

Answer any 5 questions **5 X 8 Marks=40 Marks**

1. A) List the major architectural features used in DSP system to achieve high speed program execution.
   B) For the FIR filter y(n)=(x(n)+x(n-1)+x(n-2))/3. Determine i) System Function ii) Magnitude and phase function iii) Step response.

2. A) Identify the addressing modes of the operands in each of the following instructions & their operations i) ADD B ii) ADD #1234h iii) ADD 5678h iv) ADD +*addreg
   B) Define decimation and interpolation process. Explain them using block diagrams and equations.

3. A) Write an explanatory note on direct addressing mode of TMS320C54XX processors. Give example
   B) What is the function of an address generation unit, explain with the help of block diagram of TMS320C54XX processor.

4. A) How efficient data transfer is achieved with the use of five internal buses of ADSP 2100 processor.
   B) How Black fin Processors Perform Signal Processing and Microcontroller Functions.

5. A) Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.
   B) Draw the timing diagram for memory interface for read-read-write sequence of operation. Explain the purpose of each signal involved.

6. A) Explain FFT algorithm for DFT computation? Draw signal flow graphs?
   B) With a neat block diagram explain ALU of DSP system.

7. A) Assume that the current content of AR3 is 400h, what will be its contents after each of the following. Assume that the content of AR0 is 40h.
   B) Design a data memory system with address range 000800h – 000fffh for a c5416 processor using 2kx8 SRAM memory chips.

8. Answer any **TWO**
   A) Explain how to simulate the impulse responses of FIR and IIR filters.
   B) Explain the functioning of barrel shifter in TMS320C54XX processor.
   C) Explain sequential and other types of program control.

Code No.: **54307**

MR 15 –2016-17 Admitted Students

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.-500 100.

M.TECH II SEMESTER REGULAR END EXAMINATIONS, AUGUST-2017

SUBJECT: **SENSORS AND ACTUATORS**

Branch/Specialization: **ECE/ EMBEDDED SYSTEMS**

Time: **3 Hours** Max Marks: **60**

PART-A

Answer the following Questions **5 X 4 Marks=20 Marks**

1. What are the different types of Sensors?
2. Explain about Gas Thermometric Sensors?
3. Explain about Photo Emissive Cell Photo Sensistor?
4. Explain about Filters and Converters?
5. Write a short note on Cylinders?

PART-B

Answer any 5 questions **5 X 8 Marks=40 Marks**

1. a) Explain different characteristics of Sensors /Transducers? (5M)
   b) Explain about Ultra Sonic Sensors? (3M)

2. a) Explain in detail about Spectroscopic Thermometry? (4M)
   b) Explain about Acoustic Temperature Sensor with a neat Diagram (4M)

3. a) Write down characteristics of Radiation Sensors? (5M)
   b) Explain about Fiber Optic Sensors? (3M)

4. a) Write about Data Communication with necessary Diagram? (4M)
   b) Write a short note on Automotive Sensors? (4M)

5. a) Explain about Pneumatic and Hydraulic Actuation System? (4M)
   b) Explain about Servo and Proportional Control Valves? (4M)

6. a) Write different parameters of Sensors /Transducers? (4M)
   b) Write about Noise Thermometry? (4M)

7. a) Explain about Two Capacitive Sensors? (4M)
   b) Write about Home Appliance Sensors? (4M)

8. Answer any **TWO**
   a) Write the types of Junction Semi-Conductors? (4M)
   b) Briefly explain about Strain gauge? (4M)
   c) Explain about Stepper Motors? (4M)

Code No.: **54119**

MR 15 (2016-17-Regular & 2015-16 Supply) Admitted Students

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.-500 100.

M.TECH II SEMESTER REGULAR & SUPPLEMENTARY EXAMINATIONS, AUGUST-2017

SUBJECT: **SYSTEM ON CHIP ARCHITECTURE**

Branch/Specialization: **ECE/Embedded System**

Time: **3 Hours** Max Marks: **60**

PART-A

Answer the following Questions **5 X 4 Marks=20 Marks**

1. Discuss about the components of the system?
2. Differentiate VTCMOS and MTCMOS
3. Explain standard adder cells
4. What are the different types of Interconnect Architectures?
5. Write about the SOC design approach.

PART-B

Answer any 5 questions **5 X 8 Marks=40 Marks**

1.	Write a short note on any two power dissipations	8M
2.	Explain following parameters	
	(i) Mask level measurement	4M
	(ii) Circuit level measurement	4M
3.	Explain (i) Ripple carry adder	4M
	(ii) low voltage and low power technique	4M
4.	Explain about the different SOC standard buses and architectures	8M
5.	What are the future trends and development of ROMs	8M
6.	Explain (i) Glitching power dissipation	4M
	(ii) MTCMOS circuits	4M
7.	(a) With neat diagram explain Image compression?	4M
	(b) Explain Wallace tree multiplier?	4M
8.	Discuss in detail about the different processor architecture.	8M

Code No.: **54104**

MR 15 -2016-17Admitted Students

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.-500 100.

M.TECH II SEMESTER REGULAR EXAMINATIONS, AUGUST-2017

SUBJECT: **HARDWARE SOFTWARE CO-DESIGN**

Branch/Specialization: **ECE/Embedded System**

Time: **3 Hours** Max Marks: **60**

PART-A

Answer the following Questions **5 X 4 Marks=20 Marks**

1. What are the performance criterias used in HW&SW co-design.

2. Describe the features of various application system classes.

3. Describe any one of embedded architectures in multimedia, wireless and telecommunication applications.

4. Write a short note on Compilation techniques

5. List out the features of Multi language co-simulation.

PART-B

Answer any 5 questions **5 X 8 Marks=40 Marks**

1. a). Explain a generic Co-Design methodology with a suitable diagram.
   b). Write a short notes on Distributed system co-synthesis.

2. a). Discuss the future developments in emulation and prototyping.
   b).Discuss about system communication infrastructure.

3. What is meant by compilation? Discuss about practical consideration in a compiler development environment.

4. a). Describe the following terms with respect to Hardware-software co-design
   (i).Design verification. (ii). Implementation verification.
   b). Write short notes on concurrency related to design specification and verification.

5. a).Discuss on physical realization of state variables in detail.
   b).Write short notes on concurrency in standard languages.

6. a).Explain about any two Hardware-software partitioning algorithm.
   b).Describe Weaver prototyping environment.

7. a).Explain the three principle compiler tasks.
   b).Write notes on synchronous and Asynchronous computations.

8. Answer any **TWO**
   a). Co-Design. b). Euclid's GCD Algorithm. c). Hi-level synthesis.

Code No.: **54124**

MR 15- 2016-17 Regular & 2015-16 Supply Admitted Students

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)
Maisammaguda, Dhulapally,(Post Via Kompally), Secunderabad-500 100.

M.TECH II SEMESTER REGULAR & SUPPLEMENTARY EXAMINATIONS, AUGUST - 2017

SUBJECT: **AD HOC WIRELESS NETWORKS**

Branch/Specialization: **ECE/Common to Embedded Systems (Reg) & VLSI System Design (Supply)**

Time: **3 Hours** Max. Marks: 60

PART-A

Answer All Questions **5 X 4M = 20 Marks**

1. List and explain the fundamentals of Wireless LANs.
2. Classify MAC protocols of ad hoc wireless network.
3. What do you mean by table-driven routing protocols? List examples.
4. What are the issues and Challenges in providing QoS in Ad Hoc Wireless Networks?
5. What are the various evolving Standards in sensor networks?

PART-B

Answer any 5 Questions **5 X 8M =40 Marks**

1. Differentiate HIPERLAN standards. (8M)

2. a) Explain the major issues that affect the design and performance of an ad hoc wireless network. (4M)
   b) Explain MACAW protocol. (4M)

3. (a) Explain hidden terminal problem. (4M)
   (b) Explain the AODV routing protocol. (4M)

4. a) Explain Ticket Based QoS Routing Protocol (4M)
   b) Classify QoS solutions for ad hoc wireless network. (4M)

5. a) Explain the Clustered sensor network architecture. (4M)
   b) Write briefly about data dissemination in sensor networks. (4M)

6. a. Explain about Collision Avoidance Time allocation protocol. (4M)
   b. Explain issues in designing MAC Protocols for adhoc networks. (4M)

7. a. What are the design goals of a transport layer protocol for ad hoc wireless networks. (4M)
   b. Explain one Transmission Power Management Schemes for Ad Hoc Wireless Network. (4M)

8. Answer any **TWO**
   a. Explain issues in TCP in Wireless Domain. (4M)
   b. What do you mean by flooding explain with an example. (4M)
   c. Write on Data Dissemination in wireless sensor networks. (4M)